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Wideband Airborne Early Warning (AEW) Radar

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Abstract - The Navy's Airborne Early Warning (AEW) mission has changed considerably over recent years as a result of changing threats and threat scenarios. This paper describes a radar system approach that is motivated by current and future mission considerations. The primary characteristics of the radar design include a wide operating bandwidth (1 GHz at UHF thru L-Band) for intelligent dynamic waveform agility integrated with the benefits of an electronically scanned active aperture array and a digital adaptive beamforming architecture. Proof of concept is presently underway through an ongoing research and development effort being conducted at the Naval Air Warfare Center Aircraft Division Warminster (NAWCADWAR). The effort is oriented toward a power aperture scaled roof top test bed demonstration planned for the 1994-95 time frame. Both the planned test bed performance and projected baseline full system performance are presented. In addition, brief technical descriptions of primary subsystems identifying industry participation and development status are also included.

I. Introduction

The Navy's current AEW capability is based on the APS-139 radar installed aboard the Grumman E-2C aircraft. The APS-139 radar is a low PRF system that operates at UHF with a mechanically scanned antenna implemented within a rotodome configuration [1]. The E-2C's advanced radar processing system emerged in the late 1980's and exceeded the state of airborne early warning technology. Current and future threats, threat scenarios and technological advancements support the need for a wideband AEW radar system with an electronically agile antenna beam. For example, achievements in reduced radar cross section (RCS) aircraft technology coupled with achievements in missile technology that are typical of what may be encountered throughout diverse regions of the world impose some significant challenges for the Navy's AEW mission [2]. Accordingly, the goals of future Navy AEW radar require the ability to support coastal and overland engagements, in addition to "blue water" engagements. Through the placement of emphasis on different aspects of the AEW mission, the surveillance radar community has identified UHF and L-Band operation as candidate radar operating bands that together comprise a tradeoff in meeting overall system performance objectives. Operation at UHF primarily offers detection advantages over L-Band against reduced RCS targets, and device technology that can support higher power requirements. L-Band operation primarily provides higher spatial degrees of freedom for more effective use of space-time adaptive techniques against hot clutter (multipath) and interference, in addition to better target tracking and hand over precision. The motivation toward a wideband capability with an electronically agile antenna beam primarily comes from the simultaneous consideration of RCS benefits, intelligent management of propagation phenomena, tracking and subsequent hand over performance, jamming/interference and clutter rejection, and the maturity of emerging technologies needed to realize the system's performance goals. The Naval Air Warfare Center Aircraft Division Warminster (NAWCADWAR) has been tasked to embark on a proof of concept effort under the direction of the Airborne Surveillance Block Program of the Office of Naval Technology (ONT). The proof of concept is currently based on a power aperture scaled roof top test bed demonstration; however, an airborne test bed under follow-on sponsorship is highly desirable. The goal of the test bed program is to demonstrate a wideband operating frequency capability that validates hardware and system technologies, and also provide experimental verification and support further development of radar techniques that intelligently exploit wideband adaptive phased array operation. In addition, the wideband test bed will support comparative performance evaluation of system designs that are relatively narrowband. A test bed system description is provided detailing the primary subsystems and the anticipated test bed system performance in addition to the projected performance of a full power aperture system. The technical details for each subsystem are briefly described along with the identity of responsible parties and the current status of their development effort.

II. Overall System Architecture

This section describes the overall system architecture identifying the major subsystems. The system architecture is shown in Figure 1. The system configuration involves the integration of several challenging subsystems, most of which are being custom developed. The antenna, T/R module, exciter and digital hardware subsystems are described individually in subsequent sections. The front end consists of a wideband 16 column (400-1400 MHz) dual polarized phased array antenna. The antenna array is followed by high power dual polarization column beamformers (eight elements) for each polarization. Each column is connected to a polarization select switch followed by a high power T/R module. The T/R module has a peak transmit power of 500 Watts, and an instantaneous IF bandwidth of 2 MHz on receive. Because of wideband high power device technology constraints, the T/R module design was forced to adopt a dual band transmit architecture (420-450 and 850-1400 MHz). Peacetime frequency allocation places further restrictions on wideband radiation to 420-450, 890-942 and 1215-1400 MHz. The wideband RF nucleus of the system with respect to waveform control, timing synchronization and local oscillator (LO) generation is based on the Hewlett Packard (HP) Frequency Agile Signal Simulator (FASS) housed in the exciter under system control. The FASS is planned to provide the necessary dynamic waveform agility to support the investigation of various wideband techniques of interest. The FASS generates the T/R switch control in the T/R module front end, the system master clock, the two LO's used on receive, and the RF transmit waveform that after being amplified by the RF driver, is distributed to the transmit portion of the T/R modules via the RF manifold. The system's PRF will be selectable from 0.8-10 KHz. The antenna beam on transmit is controlled via continuously variable RF phase shifters located in the transmit stage of each T/R module. The receive path of each T/R module is sampled at a low IF and provides digital I&Q data that is fed along with a second channel to one of eight digital beamformers. Each of the eight digital beamformers provide both a 2:1 channel multiplex for high speed recording in separate 32Mbyte memory modules, in addition to a 2:1 coherently summed output. The 32 Mbyte memory modules have the capacity to support experiments lasting up to 3 seconds in duration. Each of the eight summed outputs are further combined to produce sum and difference channels that are used by the near real time digital signal processor

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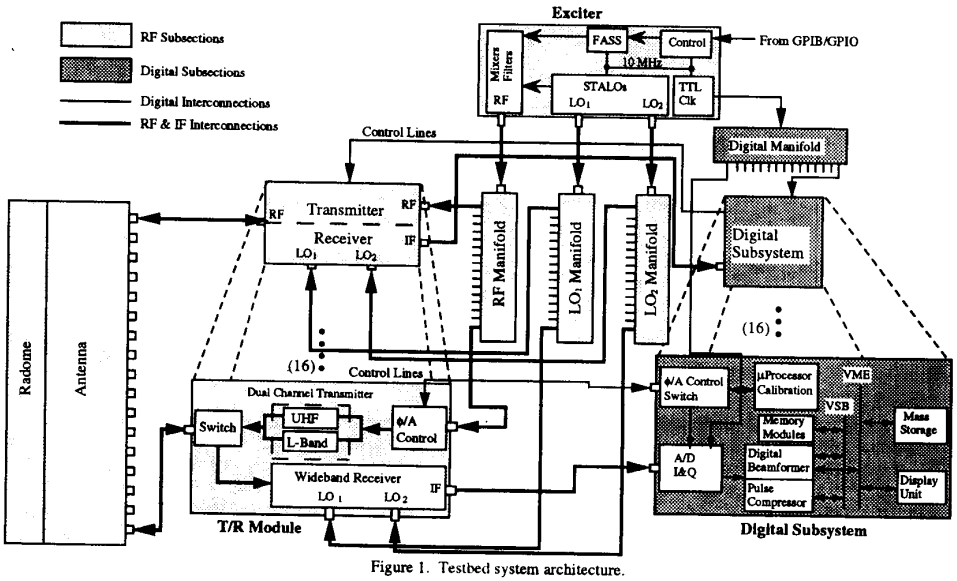

Figure 1. Testbed system architecture.

(RTDSP) to permit efficient management of the experiments and explore dynamic operation concepts. The sum and difference beams are also 2:1 multiplexed for recording in a ninth 32 Mbyte memory module. The system control unit manages the transfer of data from the nine 32 Mbyte memory modules after a data collection experiment has completed.

The test bed's digital characteristics reflect experimental data collection functionality with limited but adequate near real time utility. However, the RF characteristics represent a power aperture scaled performance envelope driven by state of the art RF hardware technology with cost considerations. Using the anticipated performance characteristics of the subsystems under development, the overall test bed's performance is estimated at three different operating frequencies using the standard radar range equation given by

$$R^4 = \frac{P_{pk}\, G^2\, N_{int}\, \sigma_t\, \lambda^2}{(4\pi)^3\, kTB_{IF}\, \overline{NF}\, L_{sys}\, L_{T/R} \left(\frac{S}{N}\right)_{1\,int}} \qquad (1)$$

where all parameters are in standard notation. Note that for test bed operation the surveillance volume search time is not important and calculations are based on coherent integration (100 pulses) being employed equally across the full operating band. The system losses L_{sys} include processing losses, antenna noise temperature losses for a T_a = 150 K, RF propagation losses, and other hardware losses not including the T/R switch losses $L_{T/R}$. The T/R switch losses are broken out separately because they are much higher than would be typical from a circulator. However, current circulator technology could not meet the system bandwidth requirements. The results are broken down and summarized in Table 1 for a P_d = 0.9 and P_{fa} = 10^{-10} against a target RCS of 5.0 m^2.

TABLE 1

TEST BED PERFORMANCE
(P_d = .9, P_{fa} = 10^{-10})

Nominal Frequency	430 MHz	900 MHz	1400 MHz
G_{ant} (one way, 60% eff)	14.91 dB	21.33 dB	25.16 dB
P_{pk} (500 watts x 16 col.)	39.03 dBW	39.03 dBW	39.03 dBW
T/R Switch Loss $L_{T/R}$	2.5 dB	2.5 dB	2.5 dB
kTB (2.0 MHz @ T = 290K)	-140.96 dBW	-140.96 dBW	-140.96 dBW
Rx NF	1.5 dB	1.5 dB	1.5 dB
Coherent Integration N_{int} (100 pulses)	20 dB	20 dB	20 dB
λ^2	-3.13 dB	-9.54 dB	-13.38 dB
$(4\pi)^3$	32.98 dB	32.98 dB	32.98 dB
σ_t = 5.0 m^2	6.99 dB	6.99 dB	6.99 dB
L_{sys}	9.5 dB	10 dB	11 dB
R	34.9 nmi	49.1 nmi	57.8 nmi

To project full system performance the surveillance volume search time must be considered. In addition, P_d and P_{fa} levels are relaxed against reduced RCS targets. For targets with RCS < ~1 m^2 the effective RCS varies proportionately to radar wavelength [3]. The projected full system performance is estimated assuming the test bed aperture is 20% of the full aperture and that each element is populated with a T/R module capable of 500 Watt peak power. Here the standard surveillance radar range equation is used given by

$$R^4 = \frac{P_{av}\, A_e\, \sigma_t\, T_s}{4\pi\, kT\, \overline{NF}\, L_{sys}\, L_{T/R} \left(\frac{S}{N}\right)_1 \Omega_{sr}} \qquad (2)$$

where the time to scan a ±360° azimuth sector fixed in elevation is given by T_s. The scan volume is given by Ω_{sr} in steradians. Note that a three face antenna configuration each having ±60° scan capability is implicit for 360° coverage. These results are broken down and summarized in Table 2 for a P_d = 0.5 and P_{fa} = 10^{-3} against a target RCS of 1.0 m^2 at UHF operation.

TABLE 2

FULL SYSTEM PERFORMANCE
(P_d = .5, P_{fa} 10^{-3})

Nominal Frequency	430 MHz	900 MHz	1400 MHz
G_{ant} (one way, 60% eff)	21.90 dB	28.32 dB	32.15 dB
P_{av} 500 watts (per el.) x 128 x 5 panels @ 20% duty	48.06 dBW	48.06 dBW	48.06 dBW
T/R Switch Loss $L_{T/R}$	2.5 dB	2.5 dB	2.5 dB
kTB (2.0 MHz @ T = 290K)	-140.96 dBW	-140.96 dBW	-140.96 dBW
Rx NF	1.5 dB	1.5 dB	1.5 dB
Ω_{sr} ($2\pi\lambda/L$); T_s=10 sec.	6.42 dB	3.21 dB	1.29 dB
λ^2	-3.13 dB	-9.54 dB	-13.38 dB
4π	10.99 dB	10.99 dB	10.99 dB
σ_t = 1.0 m^2 (scaled)	0 dB	-3.2 dB	-5.1 dB
L_{sys}	9.5 dB	10 dB	11 dB
R	323.9 nmi	314.8 nmi	297.2 nmi
Tracking Precision	Coarse	Fine	Very Fine
Propagation Degradation	High	Low	Very Low
T/R Stability	Moderate	High	High
Effective Spatial Degrees of Freedom (STAP)	Low	High	Very High

III. Antenna Array

The current antenna under development for this program is a 2-D planar array of circular disc radiators arranged in a rectangular lattice. The experimental work and the hardware fabrication is being pursued under contract with Ball Aerospace, Communications Systems Division, Boulder, CO. In addition, a theoretical Method

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of Moments analysis is being investigated both under contract with the University of Kansas Radar Systems and Remote Sensing Laboratory, Lawrence, KS, and at the NAWCADWAR.

The array is required to operate in dual linear polarization (vertical and horizontal), and maintain a minimum of 12.5 dB gain while keeping the ±60° scan loss to less than 5 dB over the entire 400-1400 MHz bandwidth. The current peak power handling requirement is 500W at each column. Early work began with the use of flared notch radiator elements because they are known to inherently possess very broad band radiation characteristics. A vertical polarization subarray was constructed and measurements revealed the presence of gain dropouts within the required operating frequency band. In addition, frequency selective surfaces were tested to increase bandwidth performance, but also fell short of the required performance. These difficulties were further complicated by additional coupling that resulted from the incorporation of horizontal polarization. The combined coupling effects caused considerable degradation of the scanned patterns off broadside as well as degraded input impedance characteristics. Consequently, the flared notch approach was discontinued, and alternate antenna elements were investigated which led to the circular disc radiator that is currently being used.

The circular disc element is etched from copper sheets printed on G-10 dielectric bonded on top of a honeycomb substrate. The ground plane is bonded to the underside of the honeycomb. The bonding agent is FM24 adhesive. The thickness of the copper (element and ground plane) is 1.4 mils, the G-10 dielectric is 5 mils and the FM24 adhesive is spread to less than 7.5 mils. The radiating face and element geometry is shown in Figure 2. The central elements (shaded) are the active elements and are driven as linear column arrays. The elements external to the shaded area are loaded with matched terminations (100Ω). The undriven rows (2) and columns (4) reduce edge effects which improved both the input impedance and the radiation performance. For the array size shown, the maximum elevation and azimuth beamwidths at 400 MHz are 44.73° and 23.73° respectively. The feed points of the array are located at every point where adjoining circles are the closest. Each feed point is fed by twin lead transitions from a microstrip balun type feed structure. The unloaded input impedance at the feed point calculated from standard microstrip theory is approximately 200Ω. The microstrip feed balun (vertical beamformer) is a Wilkinson 8:1 power divider. The losses in the vertical beamformer are -0.5 dB @ 400 MHz and -1.33 dB @ 1400 MHz. The overall antenna and feed network efficiency is expected to be approximately 60%. The original feed geometry excited all the feed points in both polarizations (see Figure 2). Figure 2(b) illustrates the original feed network. Measurements and simulation results to date have exposed undesirable input impedance characteristics over portions of the required operating bandwidth. The simulation is based on the Method of Moments (MoM) code called PATCH that was originally developed at the Sandia National Laboratories. University of Kansas modified the PATCH code to analyze circular elements, and provide radiation and input impedance characteristics for a planer array of circular disc elements [4]. The antenna model uses image theory based on an infinite ground plane and an air dielectric between the elements and ground plane. The model of the input feed network is a first order approximation to the actual feed network. The model does not include the dielectric material nor the finite ground plane edge effects. The far field patterns from the computer simulation are in reasonable agreement with the experimental measurements obtained at Ball Aerospace. Scanned patterns out to 60° off broadside track well with the measured results. The prediction of the null depths and sidelobe levels are adequate for the first sidelobe. The flexibility of the Kansas code supports numerous input parameters including disc element radius, element spacing, height above the ground plane and the feed network geometry. With the use of the Kansas code, NAWCADWAR has been investigating alternative feed configurations to improve the input impedance characteristics. One approach is shown in Figure 2(c) that consists of exciting alternate feed points. With this configuration a VSWR ≤ 2:1 at the column beamformer input is expected across the entire 400-1400 MHz frequency band. The simulation has also shown trends in input impedance as a function of ground plane spacing and feed network geometry. The simulated results will be used as an aid in finalizing the antenna design.

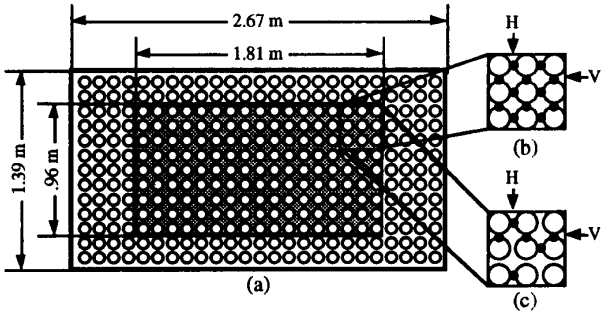

Figure 2. Array configuration (a) of the Circles array. The center shaded portion is the active section and the perimeter elements are terminated with matched loads. Also shown are the original (b) and baseline (c) feed networks indicating the feed points for the two polarizations.

IV. T/R Module and RF Component Development

The development of a wideband solid state T/R module capable of operating from 400-1400 MHz is particularly challenging. The module must be capable of producing adequate power to satisfy surveillance radar requirements while ultimately maintaining size, weight, and efficiency specifications compatible with Navy carrier-based aircraft constraints. At the time the wideband AEW program was started, such a module did not exist. However, previous wideband phase shifter and wideband amplifier developments supported by NAWCADWAR and NCCOSC (both formerly a part of the Naval Air Development Center (NADC)) resulted in a promising wideband phase shifter design [5] as well as several promising wideband transistor and amplifier designs. Nevertheless, it was concluded from a survey of state-of-the-art T/R module technology that a single contractor would not be able to adequately address a total wideband T/R module design. Therefore, a T/R module development program was initiated where the design was partitioned into four separate development efforts including a wideband phase shifter, dual band power amplifier, wideband T/R switch, and wideband receiver. The T/R module block diagram is shown in Figure 3. These components will be integrated by NAWCADWAR to provide a fully functional T/R module for rooftop test bed purposes. It is also anticipated that follow-on efforts will be required to develop an end-item airborne qualified module. A brief discussion of the salient features of each of the four T/R module subsystems as well as an overview of industry involvement and current status are given in the paragraphs that follow.

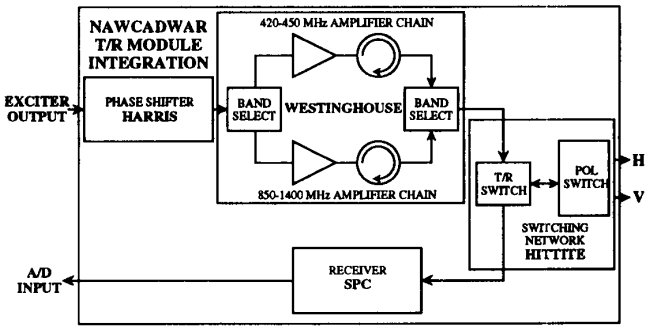

Figure 3. Wideband T/R module block diagram.

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The wideband phase shifter is currently under development by Harris Corporation, Melbourne, Florida. The design is based on the results of a development effort carried out under an earlier NAWCADWAR contract that uses a vector modulator approach [5]. The vector modulator implementation was chosen because most other traditional phase shifter designs are inherently narrow band due to their reliance on resonant circuit techniques (e.g., the use of quarter wavelength lines). The wideband phase shifter consists of two separate MMIC chips; a vector modulator chip and a variable gain amplifier chip. The vector modulator chip divides a single input signal into four orthogonal signals where the gain of each is independently controlled by a dual gate FET amplifier. The quadrature split is obtained by the use of a passive all-pass filter network followed by two differential amplifiers. The four vectors are subsequently recombined via a resistive power combiner. The phase is set by appropriately controlling the gain of adjacent quadrature vector pairs. The second MMIC chip consists of a variable gain amplifier (VGA) which provides additional output power and gain control. The VGA is also used to compensate for gain variation at the vector modulator chip output for a fixed output power application. The wideband phase shifter is used in transmit only since a digital beamforming approach is used on receive. Design specifications include ±1° phase and ±0.15 dB gain accuracy over a 10 MHz instantaneous bandwidth, 20 dB of gain control, and +10 dBm output power with at least 10 dB of overall gain. The phase shifter will be controlled by 12 bit D/A converters whose inputs are provided by calibration tables stored in local memory modules. Five D/A converters are required per phase shifter resulting from one for each of the four vector modulator dual gate FET amplifiers, and one for the variable gain output amplifier.

The power amplifier is currently being designed by the Westinghouse Electric Corporation, Baltimore, Maryland. While a single wideband transmitter is ultimately desired, fundamental bandwidth vs. efficiency tradeoffs coupled with the current state-of-the-art in power transistors has driven the design to a dual band development approach. The two bands are 420-450 MHz and 850-1400 MHz. Note that these two bands encompass three designated peacetime radar bands; low UHF (420-450 MHz), upper UHF (890-942 MHz), and L-band (1215-1400 MHz). The IFF interrogation band is also included. The primary goals for the wideband amplifier development include 500 Watts of peak output power across the band supporting maximum pulse widths and duty cycles of up to 60 μs and 20% respectively, as well as an overall amplifier efficiency of 35%. The current power amplifier design consists of a 3 watt 400-1400 MHz wideband amplifier (the power transistor for this amplifier was developed under a previous NAWCADWAR and NCOSSC program) followed by a diplexer which drives two parallel amplifier stages. The low band amplifier operates in the lower UHF band (420-450 MHz) and consists of three stages including a cascade combination of 15W and 100W UHF transistors followed by the parallel combination of two 450W transistors. The high band amplifier covers the 850-1400 MHz band and consists of preamplifier and power amplifier stages. The preamplifier stage provides gain equalization and supplies 40W to the input of the power amplifier stage. The power amplifier stage consists of a single 200W transistor driving four 200W transistors in parallel. The 200W upper UHF/L-band power transistors are being developed by the Westinghouse Advanced Technology Division and are based on an existing production die with modified input and output matching to achieve the wideband performance. These are then combined via a compensated Wilkinson power combiner to provide the 500W output requirement. Both the UHF (420-450 MHz) and upper UHF/L-Band (850-1400 MHz) amplifier stages are followed by separate circulators before being combined through an output diplexer/filter. This allows the wideband amplifier to operate into an output load VSWR much greater than the 3:1 specification. Separate circulators were selected since wideband circulators are currently heavy and bulky. Finally, the diplexer/filter is used to combine the UHF and L-band circulator outputs while also providing the harmonic suppression required to meet the -60 dBc spurious specification. The dual band power amplifier design employs an integral proprietary Westinghouse cold plate design which will be modified to provide extra real estate to mount the phase shifter, T/R switch, and receiver.

The T/R switch development was awarded to Hittite Microwave Corporation, Woburn, Massachusetts. This development consists of two separate efforts including a 500W p-i-n diode design and a 100W stacked FET design. The p-i-n diode design is intended for integration into the test-bed T/R module and is being pursued by Vectronics Microwave Corporation, Middlesex, New Jersey, under a sub-contract from Hittite. This design employs series p-i-n diodes in each of the switch arms mounted on a beryllium oxide (BeO) substrate for optimum heat sinking. Series diodes are also used to switch the 50Ω loads for matching in the receive and antenna ports. Two to three diodes are planned for use in the transmit and antenna ports to obtain the specified 40 dB of horizontal (H) to vertical (V) antenna port isolation, while four series diodes are used in the receiver port to obtain the 50 dB of transmit to receive isolation specification. Other key specifications include a 1.0 and 1.5 dB insertion loss for transmit and receive, respectively. The FET switch being pursued by Hittite is intended to provide a more suitable long term solution and is based on their stacked FET technology [6]. A FET design is ultimately desirable over the p-i-n diode configuration since it can accommodate hot switching, faster switching speeds, and draws significantly less power. The design uses a series-shunt FET stack configuration terminated by active common gate matching in both the H and V antenna ports. A single series FET stack is used in both the Tx and Rx ports, however, an extra single FET Pi configuration is used in the receive port to achieve additional isolation. Key specifications for the stacked FET switch are 100W hot switching (200W goal), and 1.9 and 2.4 dB insertion loss in transmit and receive, respectively.

The wideband receiver was awarded to System Planning Corporation (SPC), Washington, D.C. in October 1992. While the receiver design is not stressing the state-of-the-art in any particular device technology, the overall performance requirements are still quite challenging. The receiver is a double heterodyne design where up conversion is used in the first mixing stage to provide the necessary image rejection given the 1 GHz tunable bandwidth of the front end. This results in a first IF centered at 2.686 GHz with a 2.0 MHz instantaneous IF bandwidth. The output of a second and final RF mixing stage down converts the signal to an IF centered at 1.25 MHz retaining the 2 MHz bandwidth. This signal after being passed through an anti-aliasing filter is the output of the SPC receiver, and is subsequently digitized at a 5 MHz rate (minimum). Key receiver specifications include a 2.0 dB noise figure, over 68 dB of spurious free dynamic range, -15 dBm 1 dB compression point, and ±0.5 dB amplitude and ±2.5° of unit-to-unit phase tracking across the 2 MHz instantaneous bandwidth.

V. Exciter

The exciter for this system must be capable of supporting flexible waveform generation with fast switching speeds while maintaining low phase noise and spurious free performance consistent with modern surveillance radar requirements. As stated in section II, the transmit waveform and receiver LO signal integrity for the test bed radar is provided by the HP FASS. Because the FASS is based on direct digital synthesis (DDS) techniques, the necessary flexible signal generation is readily provided. However, while the phase noise and spurious free operating characteristics will satisfy the test bed requirements, they will not meet stringent detection specifications primarily due to the limited dynamic range of the D/A converters used for signal synthesis. Further improvements in this technology are expected. A conceptual diagram of the FASS is shown in Figure 4. The programmability and dynamic control of the FASS is detailed by the elements of the modulation data source. The modulation data source has AM, PM, FM, FREQ and PULSE memory locations of specified size. Access of the information stored in these waveform memories is made possible through a total of 32K sequencer memories. The FASS can be software configured to provide all three basic operating modes in the test bed architecture. The fundamental operating mode consists of loading the FASS memories prior to an experiment via the GPIB(IEEE-488) interface (Figure 5). In this mode there is no dynamic interaction during the experiment. The remaining two modes are the dynamic sequence and dynamic data modes which require the faster GPIO

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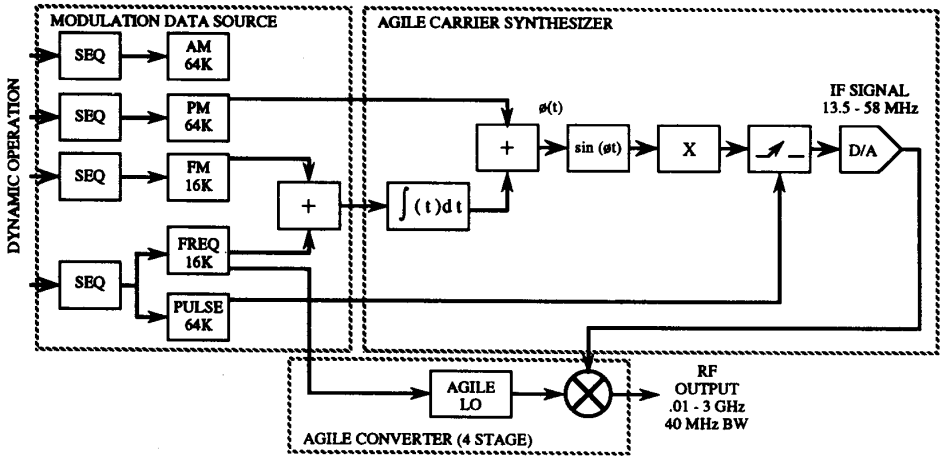

Figure 4. FASS conceptual block diagram (from Hewlett Packard Product Note 8791-3, August 1990).

interface (Figure 5). The dynamic data mode is the most versatile mode of operation, but requires extremely low level real time interaction that is processor intensive. Commercially available RTDSP's will not be able to support this mode of operation while handling basic radar processing functions, and system overhead functions. The dynamic sequence mode involves the real time selection between basic waveform packets that are stored in the FASS memories. The basic waveform packets can be combined to build a large number of different waveforms depending on their complexity subject only to the limit of 32K total sequencer memories. The test bed radar system will use the dynamic sequence mode operation via the GPIO interface to support experiments involving dynamic waveform control.

VI. Digital Control and Data Path

A functional diagram of the overall digital architecture is shown in Figure 5. The digital control and signal processing hardware is shown near the front of the array in the proximity of the T/R modules where the separate blocks in the figure partition Tx and Rx functionality. In each case separate circuitry for two channels is contained on a single board. The Tx circuitry accepts the T/R gate control and the polarization select signals and supplies them to the appropriate RF switches described in section IV. In addition, a digital transmit beam control word is accepted and decoded locally to drive the D/A converters used by the Harris RF amplitude and phase circuitry. The source of these signals can be provided by either the system controller or the near RTDSP via the VME bus to allow flexible experiment design and not preclude dynamic decision operation. On the receive side the video output of each module is digitized by the Burr-Brown ADC-603 12-bit A/D converter operating at a 5 MHz minimum rate. The output of the A/D converters are passed through digital I&Q circuitry to form separate 12 bit I&Q data words at a 1.25 MHz rate [7]. The words are transmitted for pairs of channels serially to digital beamformer (DBF) circuit boards using differential line drivers for noise immunity. Each of the eight DBF circuit boards perform a coherent summation of the two input channels, and provide a 2:1 multiplex for the high speed recording of raw channel data. Before recording and coherent summation the raw 12 bit I&Q data words are first passed through 15 tap FIR filters spaced at 1.25 MHz for channel calibration. The DBF circuits run at a 20 MHz system clock rate provided by the FASS, and perform a synchronous data transfer via a dedicated 20 Mbyte/sec VSB bus to a 32 Mbyte memory module. The eight DBF circuit boards are configured as four master-slave pairs. The master DBF circuits accept a slave output (two channels coherently combined) and coherently combines it with its own (two channels coherently combined) to effect a four channel coherent summation. Each of the four master DBF circuit outputs are supplied to the real time processor (RTP) summer circuitry. The RTP summer circuitry coherently combines the remaining four channels and forms I&Q multiplexed sum (+) and difference (-) beams for the pulse compressor (PC) circuitry. The PC circuitry consists of two 90 tap programmable filters whose sum and difference beam range compressed outputs are 2:1 multiplexed for both high speed recording and supply to the RTDSP. The DBF, RTP summer and PC circuitry are being developed at the Naval Research Lab (NRL) in support of this effort. The RTDSP is planned to have the capability to accept data via the 20 Mbyte/sec VSB bus, although the data is also planned to be available via the 5 Mbyte/sec VME bus for possible work station use. Once an experiment has been completed, the nine 32 Mbyte memory modules are serially down loaded to tape storage via the VME bus and the recorded data is available for off-line processing. The memory down load procedure will take approximately one minute at a 5 Mbytes/sec. rate. For baseline operation, the system controller will down load instructions to the FASS via the VME bus GPIB interface for static experiment operation. To support more sophisticated dynamic operation, the FASS will be software configured to allow real time dynamic pulse to pulse waveform control via the GPIO interface located in the RTDSP using the dynamic sequence mode. This type of operation will be RTDSP intensive since a number of other system control functions must also be handled in real time. However, the performance of commercially available RTDSP's will allow considerable flexibility. The RTDSP design is still in its early stages.

VII. Wideband Techniques

A smaller effort encompassed by the AEW Wideband Test Bed Program is the development of wideband techniques that take advantage of the test bed's performance characteristics. Although some of the work performed under this task has broader application, the largest portion of the effort is focused on the use of the test bed to support the testing and development of various processing techniques once it becomes operational. The wideband techniques effort has been subdivided into three smaller areas that are being pursued in a prioritized manner. In a decreasing order of priority they consist of dynamic management of classical waveform parameters and antenna beam control, space-time adaptive processing methods and advanced signal processing concepts. The dynamic management of classical waveform parameters is made possible through the flexibility of the FASS. This area primarily involves channel characterization and intelligent clutter management, wideband frequency hopping for multipath null avoidance and detection enhancement while search, and the use of detection cued waveforms for faster revisit (track) and longer dwell (possible i.d.). For example, frequency hopping can be managed to not only avoid nulls caused by propagation, but also theoretically provide up to 12 dB of two way signal enhancement. In addition, detection cued step frequency waveforms may be employed at high PRFs to minimize compensation of target range walk effects, and provide high range resolution signatures useful for target identification. The potential benefits of space-time adaptive methods have been widely recognized by the surveillance radar community and will undoubtedly be utilized in next generation Navy AEW. Considerable effort is underway outside this program to identify and/or develop space-time adaptive algorithms that address Navy

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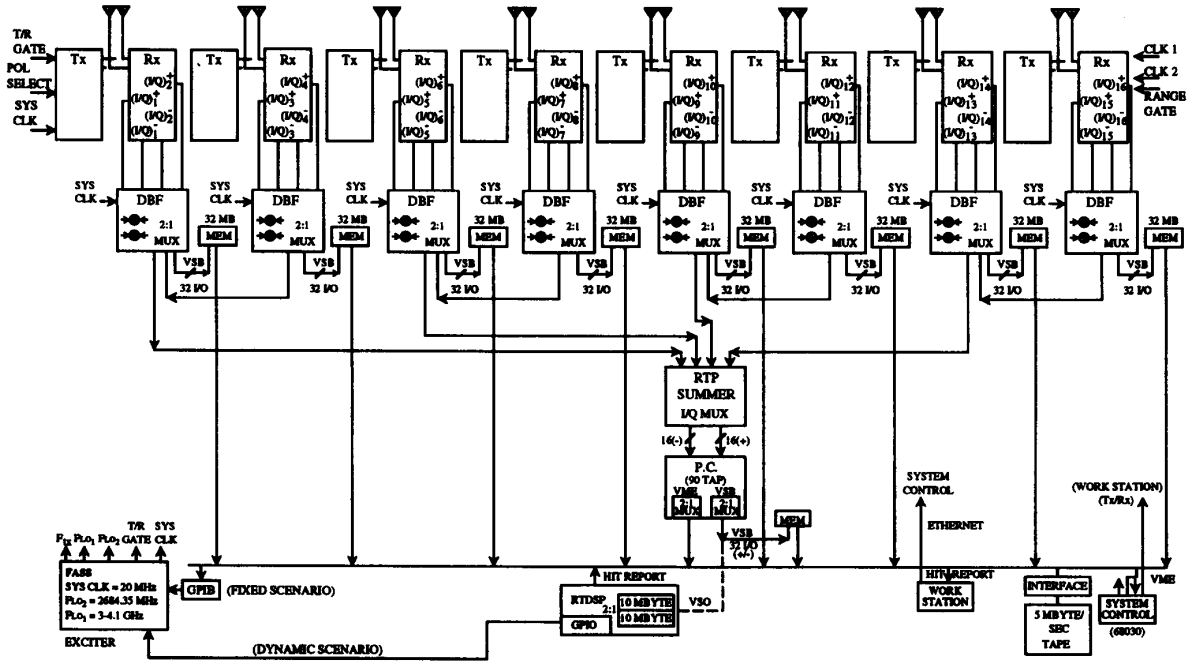

Figure 5. Digital subsystem architecture.

mission needs. Once the test bed radar becomes operational it is intended to be used as a hardware vehicle to exercise these algorithms and support performance evaluation. Under this program, the use of extremely fine programmable true time delay applied at carefully chosen points in the array is being examined to provide a limited number of wideband degrees of freedom. Advanced signal processing concepts under investigation include Gaussian pulse shaping that uses classical and wavelet concepts for enhanced detection and identification [8].

VIII. Demonstration Schedule

Work on the wideband AEW test bed began in the middle of 1989 with an original schedule leading to demonstration by late 1994. Due to funding/manpower constraints and technological challenges, the original schedule has been delayed by approximately one year. The wideband subarray hardware, system/beamsteering controller, digital beamformer and wideband exciter subsystems will be delivered and tested in the third to fourth quarter of 1993. The wideband transmit amplifier, phase shifter and switch circuitry will be delivered and tested by the third quarter of 1993, and the wideband receiver will be delivered and tested in the second quarter of 1994. The T/R module components will be integrated into 20 T/R modules and tested in the fourth quarter of 1994, as will the cooling system and T/R module digital subsystems. Overall test bed integration and checkout is scheduled for the second quarter of 1995 with an operational demonstration planned for the second half of 1995. Frequency allocation has already been approved.

IX. Concluding Remarks

This paper describes a wideband test bed radar system under development at NAWCADWAR to support next generation Navy AEW. The technology challenges associated with key subsystems have been highlighted along with development status. It is anticipated that once the test bed radar system becomes operational, it will be a significant asset that will support ongoing development efforts that include wide operating bandwidth for dynamic waveform agility integrated with an electronically scanned active aperture array, and a digital adaptive beamforming architecture .

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